REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. New claims 15 and 16 are added. Claims 1-16 are pending in this application.

Double Patenting

Claims 1-14 stand rejected under the judicially created doctrine of double patenting over claims 1-5 of U.S. Patent No. 6,647,433. If this rejection is maintained, Applicant will file a terminal disclaimer upon receiving an indication of allowability of claims 1-14.

35 U.S.C. § 102

Claims 1-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,109,190 to Sakashita (hereinafter "Sakashita"). Applicant respectfully submits that claims 1-14 are allowable over Sakashita.

Sakashita is directed to a test circuit device for facilitating a connection test in and between integrated circuits (see, col. 1, lines 8-11). The apparatus of Sakashita includes a circuit block, a plurality of boundary scan registers, a system data terminal, a test signal terminal and a control circuit (see, Abstract). The control circuit responds to a test signal to generate control signals for controlling the boundary scan registers, which are connected in cascade to each other and each connected to the circuit block (see, Abstract).

In contrast, with respect to claim 1, claim 1 (emphasis added) is directed to a method comprising:

> issuing one or more command(s) to one or more inputs of a general purpose input/output (GPIO) system, wherein the command(s) cause a first output of the GPIO system associated

with a first input of the inputs to issue a control signal to a latch associated with a **port bypass circuit (PBC)**, and a second output of the GPIO system associated with a second of the inputs of the GPIO system to issue a clock signal to a latch associated with a PBC addressed by the received command(s); and

setting the state of the PBC with the received control signal if the control signal and the clock signal are consistent to change the state of the PBC.

Applicant respectfully submits that the method of claim 1 is not disclosed by Sakashita.

Applicant respectfully submits that no port bypass circuit (PBC) as recited in claim 1 is disclosed in Sakashita. As discussed in Applicant's specification, port bypass circuits are used as a reliable means of switching to selectively couple network elements (see, for example, page 1, line 15 – page 2, line 24). Although Sakashita does disclose, as pointed out in the July 7, 2005 Office Action, a bypass register 8a (in Figs. 1 and 5), this bypass register is not a port bypass circuit. The bypass register of Sakashita receives test data TDI through a test access port TAP, and outputs data to the multiplexer 8f of Sakashita (see, col. 7, lines 54-58, and col. 9, line 67 – col. 10, line 9). Applicant respectfully submits that the receiving and outputting of test data as performed by the bypass register of Sakashita does not disclose or suggest selectively coupling network elements as performed by a port bypass circuit. As described in Sakashita, the bypass register simply holds data (the test data TDI) – there is no discussion in Sakashita of this test data being used for switching or selectively coupling network elements. As such, Applicant respectfully submits that Sakashita does not disclose the port bypass circuit of claim 1.

Thus, for at least these reasons, Applicant respectfully submits that Sakashita does not disclose the method of claim 1. If this rejection is maintained, Applicant respectfully requests that the Examiner specifically

identify by its reference number(s) which component(s) of Sakashita teaches a port bypass circuit.

With respect to claims 2-6, given that claims 2-6 depend from claim 1, Applicant respectfully submits that claims 2-6 are allowable over Sakashita for at least the reasons discussed above with respect to claim 1.

With respect to claim 7, Applicant respectfully submits that, analogous to the discussion above regarding claim 1, Sakashita does not disclose a port bypass circuit as recited in claim 7, and that claim 7 is thus allowable over Sakashita.

With respect to claim 8, Applicant respectfully submits that, analogous to the discussion above regarding claim 1, Sakashita does not disclose a port bypass circuit as recited in claim 8, and that claim 8 is thus allowable over Sakashita.

With respect to claim 9, claim 9 is directed to a method comprising:

> issuing one or more control command(s) to a controller which, when interpreted causes the controller to issue control signals to a port bypass circuit to control an operational state of the port bypass circuit; and
> verifying that the controller accurately received the one or more control commands before the control signals are passed to the port bypass circuit.

Applicant respectfully submits that no such issuing and verifying is disclosed in Sakashita.

As discussed above regarding claim 1, Sakashita does not disclose a port bypass circuit as recited in claim 9, and thus Sakashita cannot disclose the controller to issue control signals to a port bypass circuit to control an operational state of the port bypass circuit as recited in claim 9. Furthermore, as there is no port bypass circuit disclosed in Sakashita, there cannot be any verifying that the controller accurately received the one or more control

commands before the control signals are passed to the port bypass circuit as recited in claim 9.

Thus, for at least these reasons, Applicant respectfully submits that Sakashita does not disclose the method of claim 9.

With respect to claims 10 and 11, given that claims 10 and 11 depend from claim 9, Applicant respectfully submits that claims 10 and 11 are allowable over Sakashita for at least the reasons discussed above with respect to claim 9.

With respect to claim 12, Applicant respectfully submits that, analogous to the discussion above regarding claim 9, Sakashita does not disclose the issuing and verifying of claim 12. Accordingly, Applicant respectfully submits that claim 12 is allowable over Sakashita.

With respect to claim 13, Applicant respectfully submits that, analogous to the discussion above regarding claim 1, Sakashita does not disclose a port bypass circuit as recited in claim 13, and that claim 13 is thus allowable over Sakashita.

With respect to claim 14, given that claim 14 depends from claim 13, Applicant respectfully submits that claim 14 is allowable over Sakashita for at least the reasons discussed above with respect to claim 13.

Applicant respectfully requests that the §102 rejections be withdrawn.

New Claims

New claims 15 and 16 are added.

With respect to new claim 15, new claim 15 depends from claim 1 and Applicant respectfully submits that new claim 15 is allowable over the cited references for at least the reasons discussed above with respect to claim 1.

Furthermore, Applicant respectfully submits that the cited references do not disclose or suggest a method according to claim 1, wherein setting the state of the PBC comprises forwarding, to the PBC, the control signal issued to the latch as recited in new claim 15.

With respect to new claim 16, new claim 16 depends from claim 13 and Applicant respectfully submits that new claim 16 is allowable over the cited references for at least the reasons discussed above with respect to claim 13. Furthermore, Applicant respectfully submits that the cited references do not disclose or suggest a storage system according to claim 13, wherein the latch is to latch the control signal to the PBC only if the first input and the second input receive the command unchanged as recited in new claim 16.
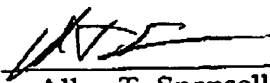
Thus, Applicant respectfully submits that new claims 15 and 16 are allowable over the cited references for at least these reasons.

Conclusion

Claims 1-16 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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